Self-Consistent GaAs FET Models for Amplifier Design and Device Diagnostics

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Abstract—**A procedure has been developed for producing accurate and unique small-signal equivalent circuit models for carrier-mounted GaAs FET's. The procedure utilizes zero drain–source bias S-parameter tests to determine accurate values of carrier parasitics, and dc measurements to evaluate the FET's gate, source, and drain resistances. Subsequent S-parameter measurements at full bias are then used to resolve the FET into an equivalent circuit model that has only 8 unknown elements out of a possible 16. A technique for evaluating the frequency range of accurate data is presented and the FET model shown is useful well above the maximum frequency of measurement. Examples of device diagnostics are presented for RCA flip-chip mounted GaAs FET's.**

I. Introduction

AN ACCURATE DEVICE model based on the measurement of completed wafers is an invaluable tool for device and amplifier development. Characterization of the intrinsic and parasitic structure of the FET can be used to assess the impact of process and mask variations on device performance. For instance, the effects of varying gate location and recess depth, source and drain widths, gate metallization thickness and composition, could be directly measured. For amplifiers, modeling can be used to predict device scattering parameters (S-parameters) at millimeter-wave frequencies where they cannot be measured with current commercial equipment. Within the measurement range of network analyzers, these accurate models can effectively be used to simulate the performance of matched and combined FET cells to determine optimal circuit topology.

Previously, attempts to try to construct FET models were based only on S-parameter measurements. But Vaitus [1] has shown that the errors associated with measuring and de-embedding device scattering parameters leads to significant errors in the equivalent circuit element values for GaAs FET's. Some of these errors can be reduced with improved S-parameter measurement techniques such as the through, short, delay (TSD) approach [2] and the technique of Bianco *et al.* [3], wherein the effects of RF launchers are accurately removed. However, GaAs power FET's are carrier-mounted and therefore are surrounded by more parasitic circuit elements and require additional de-embedding.

Part of the problem is that there are too many variables to create a unique solution based only upon a set of broad-band S-parameter measurements. The situation is even worse for characterization of GaAs dual-gate FET's. Tsironis and Meierer [4] attempt to resolve 28 circuit element values from 3-port S-parameter data. As they discuss, the optimization process is hopeless unless started with accurate estimates of most circuit element values from independent measurements or calculations.

In this paper, an accurate and unique equivalent circuit model is developed by using three different automated measurements of the carrier-mounted FET.

1) The FET mounted in its carrier is measured from 4–20 GHz using a coaxial test fixture where the chip is only a connector away from the measurement reference plane where the calibration occurs. A recent improvement in this technique is the use of electrically short 3.5-mm connectors. These connections are SMA compatible, low loss, and resonance free to 34 GHz.

2) The gate (R_g), source (R_s), and drain resistances (R_d) are measured using an automated Fukui approach [5].

3) Cold FET S-parameter measurements with zero drain-to-source voltage are used to determine external parasitics such as wirebound inductance and carrier stand-off capacitance (these measurements must be made just before the hot S-parameter tests).

With these additional measurements the number of unknown variables is reduced from a total of 16 to 8, which makes it much easier to determine an accurate and unique model for the FET chips that fits the measured data.

Once the modeling procedure has been established, models are developed for RCA flip-chip FET's with submicrometer T-shape gates [6]. The range of validity of the model, convergence considerations, and the diagnostic information obtained for these wafers are discussed.

II. Dummy Package Measurements

S-parameter measurements were made of 1.4-mm-wide carriers without FET chips, as shown in Fig. 1. The reference planes are the sides of the carrier as in the case of the device measurements. The S-parameter data for the ATC-S capacitors (used as stand-offs) showed that the RF capacitance was very close to one half of the value measured by a low-frequency bridge and well behaved up to 18 GHz.

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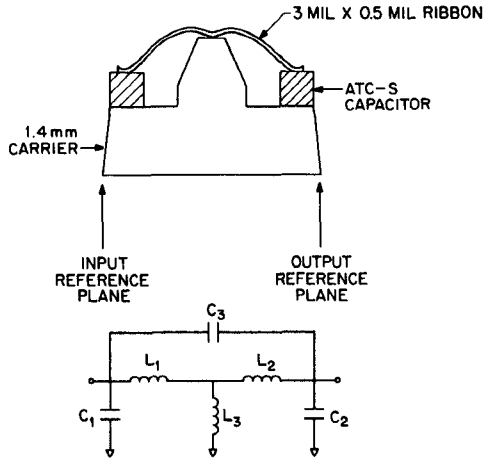

Fig. 1. FET carrier model (lower) and cross-sectional view of carrier (upper).

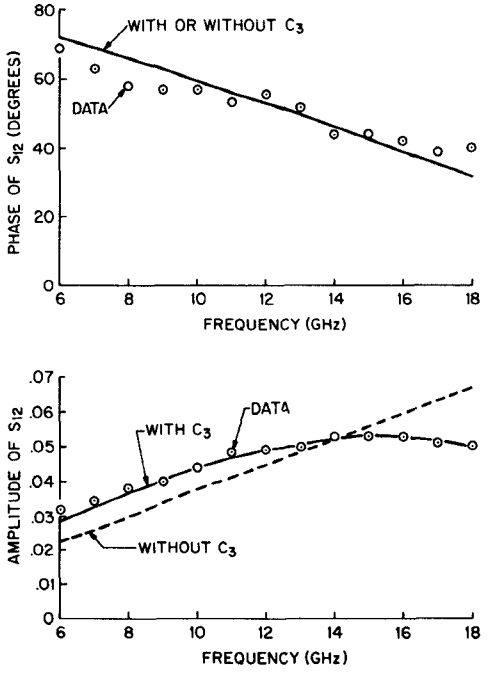

Fig. 2. Amplitude and phase of S_{12} as a function of frequency for the FET carrier.

The lumped-element model shown in the lower part of Fig. 1 provides the best agreement with the S-parameter data for the dummy carrier (i.e., package). The program SUPER-COMPACT [7] was used to optimize the element values for best agreement with the data. The ribbon lengths on the two sides are slightly different, but are nominally 0.38 mm. This should produce about 0.20-nH inductance, which is close to the values measured ($L_1 = 0.207$ nH, $L_2 = 0.168$ nH). These data show that the pedestal inductance L_3 is approximately 20 pH for a pedestal height of 0.30 mm. Fig. 2 shows the amplitude and phase of S_{12} for both the model and the measured data. The agreement is seen to be excellent for the model which C_3 is included.

To further study mounting parasitics, other FET carriers were assembled and S-parameters were measured from 4 to 20 GHz. Table I shows the characteristics of each and the optimized values of the equivalent circuit components.

TABLE I
EQUIVALENT CIRCUIT PARAMETERS FOR DUMMY MESFET CARRIERS ($C_1 = C_2 = 0.04$ pF)

Carrier Width (mm)	Pedestal Height (mm)	Feature	L_1 (nH)	L_2 (nH)	L_3 (pH)	C_3 (pF)
1.4	.30		0.207	0.168	20.0	0.018
1.78	.30		0.224	0.249	19.1	0.011
1.78	.30	3 Ribbons	0.152	0.162	19.7	0.014
1.78	.125		0.295	0.313	28.3	0.010
1.78	0	Weld	0.180	0.251	17.5	0.011
1.78	0	Epoxy	0.253	0.236	22.8	0.010

It is interesting to note that the pedestal inductance (L_3) measured for the three carriers with 300-μm-high pedestals is the same value to within 5 percent. L_3 is present even for the zero-high pedestal. This implies that some pedestal inductance results from mutual inductance between the gate and drain leads. The geometry of the bond leads in the pedestal region may thus be important in determining the pedestal inductance.

The stability factor K for an FET is defined as

$$K = \frac{1 + |S_{11}S_{22} - S_{21}S_{12}|^2 - |S_{11}|^2 - |S_{22}|^2}{2 \cdot |S_{12}| \cdot |S_{21}|}.$$

A lossless network has a unity value of K. Since we observed K values much larger than unity in the tests on the dummy carriers, we believe there are losses associated with the carrier itself. These losses may arise due to power dissipation in resistance but it is more likely that they result from radiation loss.

The agreement between the S-parameters calculated for the dummy carrier models and the experimental data is improved if some small loss is assumed in the wire ribbons and stand-off capacitors. The agreement between S-parameters for the carrier-mounted FET's and their model is improved slightly with the addition of carrier loss.

III. Zero-Bias Measurements

As Diamond and Laviron [8] have suggested, the S-parameter measurements for a device with $V_{ds} = 0$ V permits more accurate evaluation of device parasitics because the equivalent circuit is much simpler. Fig. 3 shows the lumped-element equivalent circuit of the carrier-mounted FET for the case of zero biasing. Using S-parameter data for device B1824-20C from 4 to 18 GHz, all circuit element values were optimized for a minimum calculated error function in the program SUPER-COMPACT. For small differences in the error function, the optimum values of R_g, R_s, and R_d vary widely depending upon the optimization method and the starting values. For example, R_s varied between 0 and 0.7 Ω, R_g varied between 0.9 and 1.53 Ω, and R_d varied between 0.5 and 1.3 Ω. Clearly, the value of $R_s = 0$ Ω is nonphysical as one expects R_s to be very nearly the same as R_d due to the construction of the device. It is interesting to note that the values of L_s, L_d, L_g, R, and C did not vary more than ± 1 percent for these cases even with widely varying resistance values.

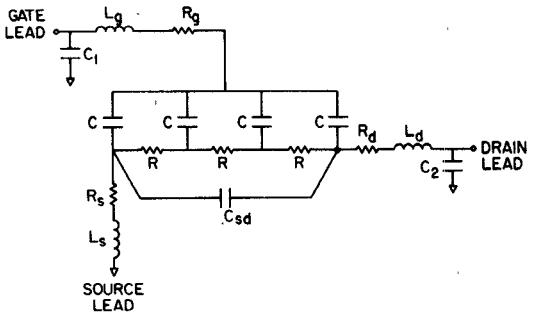

Fig. 3. Equivalent circuit of carrier-mounted FET at zero drain-source bias voltage.

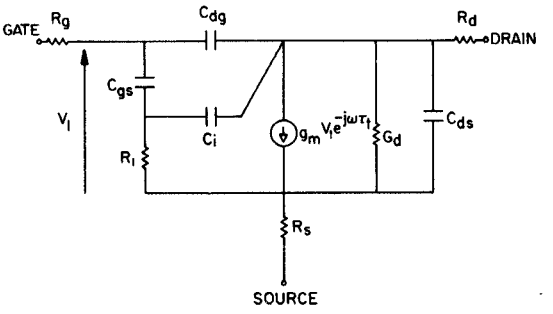

Fig. 4. FET chip equivalent circuit at normal operating bias.

TABLE II
OPTIMIZED CIRCUIT ELEMENT VALUES FOR FET 1824-20C WITH $V_{ds} = 0$ V FOR 4–18 GHz RANGE WITH $R_g = 0.549\ \Omega$, $R_s = 1.048\ \Omega$, $R_d = 1.367\ \Omega$, $C_1 = 0.044$ pF, $C_2 = 0.039$ pF

V_{gs} (V)	R (Ω)	C (pF)	C_{sd} (pF)	L_g (nH)	L_d (nH)	L_s (pH)
0.	.3354	.2289	.1730	.3115	.2514	10.71
-1.	.5143	.1814	.1726	.3134	.2507	10.73
-2.	.7593	.1620	.1725	.3158	.2516	10.48

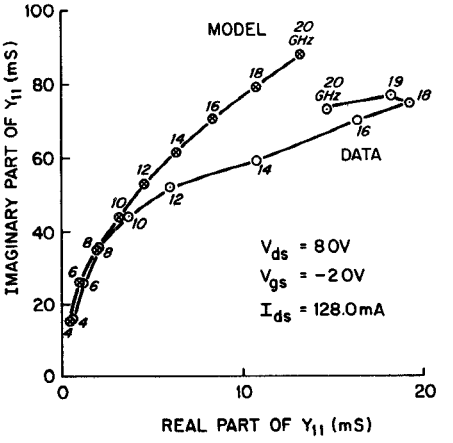

Fig. 5. Admittance parameter Y_{11} as function of frequency for the FET chip and for the de-embedded data.

To resolve this accuracy problem, we use resistance values determined from dc measurements of the type described by Fukui. These resistance values give the best approximation available. Using these values, Table II shows the values of the other circuit elements for three values of V_{gs} for $V_{ds} = 0$. The values of R and C vary with gate bias as expected and the inductive circuit elements vary less than 2 percent. The calculated S-parameters for this optimized model are extremely close to the measured data. The values R and C are not used for subsequent modeling at full bias but may be used for diagnostic information about the gate and the conduction channel.

IV. FET Modeling at Full-Bias Voltage

Subsequent S-parameter measurements at full operating bias can then be used to resolve the FET chip into an RF equivalent circuit of the type shown in Fig. 4. Using this procedure, the final FET model has only 8 unknown elements (in the FET chip) out of a possible 16 (in the carrier-mounted FET). This circuit model has several important advantages over other configurations. The internal feedback capacitor C_i physically results from drain-to-channel feedback and causes the reverse transfer conductance (i.e., drain-to-gate) to have positive sign and square-law frequency dependence. This behavior is also observed in our two-dimensional simulation [9] as well as in laboratory measurements. The current source is controlled by the total voltage across the (gate) capacitor C_{sg} and the (channel) resistor R_i rather than by the voltage across C_{sg} alone. This forces the time-delay factor τ_t to account for all delay effects under the gate and permits the value of R_i to be based only upon input loss. By comparison of the Y-parameters of the chip's equivalent circuit model with those of an accurate two-dimensional FET model [9], we find the equivalent circuit model to be accurate to about 50 GHz.

As discussed earlier, the resistance values R_g, R_s, and R_d are obtained from Fukui measurements and inductance value are obtained from the $V_{ds} = 0$ measurements. Values of the FET circuit elements are optimized for best agreement with the experimental data. It is interesting to compare the Y-parameters of the FET chip model with experimental data. The experimental Y-parameters are obtained by de-embedding the device from the carrier at each RF frequency. In all cases, the inductances used are fixed and equal to the values obtained from zero drain-source bias measurements.

Fig. 5 shows the comparison of the model and data for Y_{11} for device B1824-20C. The agreement becomes progressively worse as frequency is increased and the functional behavior of the experimental data with frequency is nonphysical above 18 GHz. The parameters Y_{21} and Y_{22} show similar behavior. This departure from the theoretically expected behavior means that only data up to 18 GHz are accurate. Notice that the actual error between the data and final model is not large; the horizontal scale has been expanded for clarity in Fig. 5. The model was optimized for the frequency range 6–18 GHz. Optimization over a larger (or smaller) range does not change the functional form of the Y-parameters.

Fig. 6 shows the Smith Chart values of S_{11} and S_{22} computed using the FET model (including the carrier) and

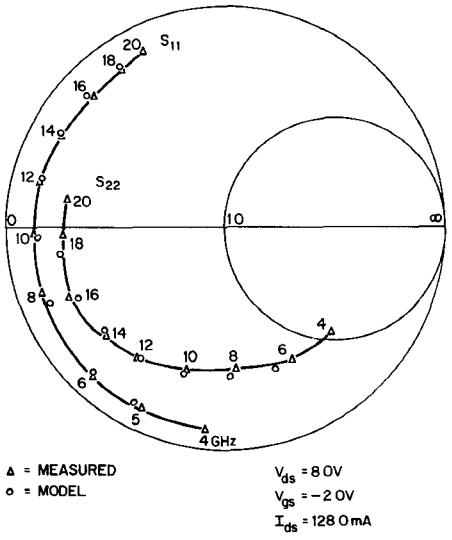

Fig. 6. Smith Chart display of measured data and model for S_{11} and S_{22} for the carrier-mounted FET.

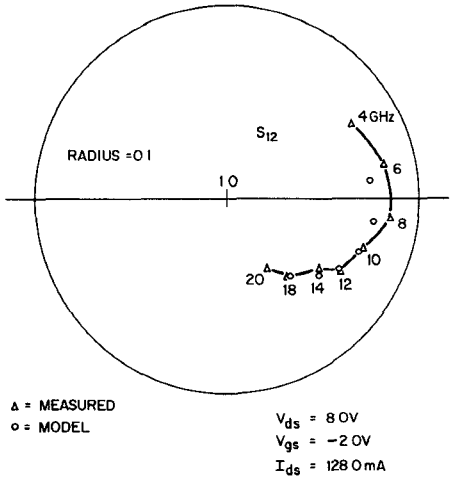

Fig. 7. Smith Chart display of S_{12}.

the measured data. The errors are clearly more apparent in Fig. 5 than in Fig. 6. Figs. 7 and 8 show S_{12} and S_{21}, respectively. Errors are small. FET's measured and modeled a second time (after disassembly from the test fixture) show only small changes in the values of equivalent circuit elements. Table III shows the percentage change in each circuit element value. The circuit elements R_i and C_i are not well resolved by the data set but do not affect the maximum available gain (MAG) greatly. Notice that f_t, f_{MAX}, and K are not greatly changed upon remeasurement.

V. Convergence Considerations

SUPER-COMPACT is extremely useful for evaluating the values of the equivalent circuit for best agreement with the measured data. However, some element values are not uniquely determined and the resulting value is a function of the search technique. We have addressed this problem by minimizing the number of elements permitted to vary. Using the procedures described earlier, our final FET model has only 8 variable elements, out of a total of 16.

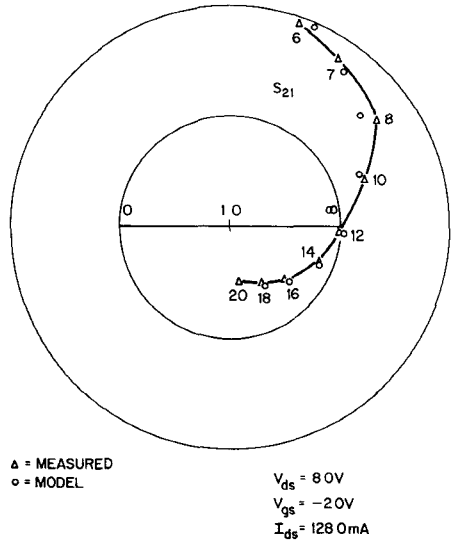

Fig. 8. Smith Chart display of S_{21}.

TABLE III
Equivalent Circuit Element Values for Two Separate Measurements of Two FET's and Percentage Changes (Data Used for 6–18 GHz with $V_{ds} = 8$ V, $VV_{ds} = -2$ V)

FET	I_{ds} (mA)	g_m (ms)	τ (ps)	G_d^{-1} (Ω)	R_i (Ω)	C_{gs} (pF)	C_i (fF)	C_{dg} (fF)	C_{ds} (fF)	f_t (GHz)	f_{max} (GHz)	K
B 1499 97	95 0	46 99	8 186	326 2	2 274	0 7385	46 6	25 87	71 4	10 1	35 0	2 23
Remeasured	95 0	42 70	8 074	312 3	2 500	0 6874	47 0	22 81	67 3	9 9	34 3	2 30
B1824 200	128 0	42 27	7 405	376 4	1 088	0.6870	10 0	41 57	190.0	9 8	35 2	2 05
Remeasured	127 0	39 88	7 944	359 0	1 330	0 6631	14 9	40 42	193 0	9 6	33 2	2 06
Avg % Change, Remeasured		8 0	4 4	4 7	16 0	5 5	25 0	7 9	3 9	2 0	4 0	1 8

The problem of unequivocally determining the optimum values of the equivalent circuit elements is not trivial. After extensive investigation, we have found that:

1) optimization should be done with the fewest possible unknown circuit elements;

2) both random number of gradient search techniques should be used to assure that the results are convergent and independent of the starting values;

3) some circuit element values may never converge for certain data sets;

4) convergence of the important circuit elements occurs early in the search.

VI. Evaluation of f_{MAX}

The frequency of 0-dB maximum available gain (MAG) f_{MAX} is often evaluated using analytical expressions derived with simplifying assumptions. The most accurate value is obtained by extrapolating the FET chip model (i.e., the de-embedded chip), in frequency using SUPER-COMPACT because the simplifying assumptions are often not valid for real devices. For accuracy, it is necessary to achieve good agreement between the model and data for the stability factor (as well as for S-parameters) over the range of measurement. MAG strongly depends upon the stability factor.

Fig. 9 shows an example of the effect of carrier losses for an FET of 600-μm periphery from wafer B1824. The figure

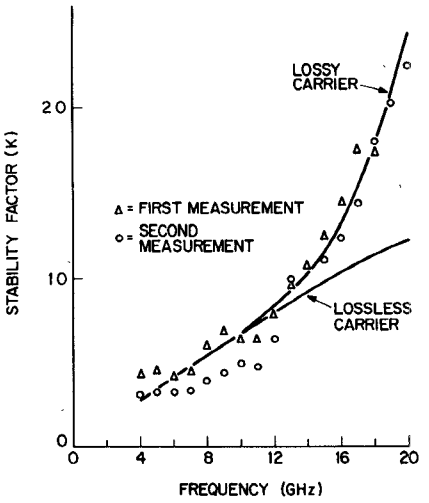

Fig. 9. Stability factor as a function of frequency for the measured data and for the models.

shows the stability factor obtained from the data for two separate measurements and from the model for the MESFET carrier with and without loss. The agreement is seen to be better for the lossy carrier. The optimum value of added loss is 100 Ω in series with capacitors C_1 and C_2 shown in Fig. 1. The value of f_{MAX} obtained for the chip alone for either case is 34.0 GHz. However, for some cases, the addition of loss to the carrier improves the model such that the value of f_{MAX} is altered.

VII. Diagnostic Information Produced by Models

A group of GaAs FET's from six different wafers were characterized to determine the relationship between device parameters and RF performance. All devices are flip-chip mounted and have 600-μm source periphery and approximately 1-μm gate length. The dc parameters were measured using the automated Fukui method, and S-parameter measurements were made by our method from 4 to 20 GHz. Lumped-element circuit models were constructed for each device using the procedure described. We present a summarized version of this data for comparison of the wafers.

Table IV shows results from several devices from six wafers. The Fukui pinchoff voltage is measured at small drain-source voltages in the linear regions and is always less than that measured above current saturation. The average $N \cdot a$ product (donor-thickness product) is obtained by averaging the value from the Fukui measurement (from maximum dc channel currents) and the value from RF capacitance measurements. The errors involved in determining the $N \cdot a$ product from the Fukui data alone make the value smaller while the errors involved in the RF measurement make the value large. The average of these $N \cdot a$ values is thus more accurate.

The average donor value N is calculated from the average $N \cdot a$ product and the pinchoff voltage. The donor values calculated in this manner are generally larger than measured in profiling the wafer but are believed to be more accurate because they are more compatible with device performance.

TABLE IV
Summary of DC and RF Test Results for 12 FET's
(RF Tests Made at $V_{ds} = 8$ V, $V_{gs} = -2$ V)

Device	Fukui Pinch-Off (V)	Average N·a (10^{12}cm^{-2})	Average N (10^{17} cm^{-3})	f_t (GHz)	f_{MAX} (GHz)	f_{3db} (LS) (GHz)
B1271-A54	3.68	3.45	1.9	12.7	41.2	32.3
B1824-1C	4.94	4.12	2.2	9.8	36.0	26.5
-4C	5.56	4.02	1.9	10.3	34.0	27.0
C1851-11	4.35	3.89	2.2	10.1	34.4	22.0
-3	3.0	3.35	2.2	12.0	36.0	25.0
B1512-1A	2.5	4.26	4.0	9.0	32.0	22.6
-2A	3.5	4.15	2.9	8.75	32.0	22.0
E627-64	6.27	4.05	1.7	8.75	32.5	18.0
-65	6.11	3.85	1.6	8.80	32.0	18.5
-2	5.0	3.75	1.8	10.0	32.0	21.6
B1832-17	5.62	5.1	3.0	7.7	30.5	17.5
-16	5.81	5.7	3.0	8.0	29.8	17.6

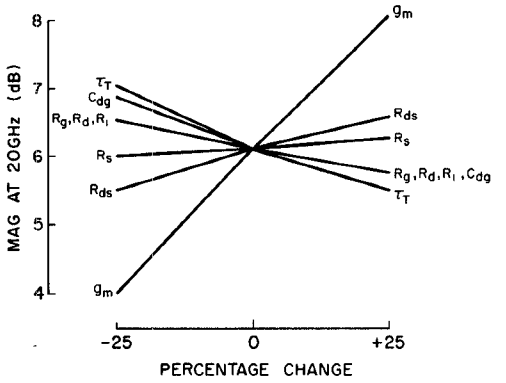

Fig. 10. Maximum available gain as a function of percentage change in value of model elements for FET B1824-20C at $V_{ds} = 8$ V, $V_{gs} = -2$ V.

The current cutoff frequency f_t is calculated from the ratio of transconductance to gate-source capacitance using the equivalent circuit model. The f_{MAX} is obtained by extrapolating the FET chip model in frequency using SUPER-COMPACT. Finally, f_{3db} (LS), the frequency of 3-dB maximum available gain under optimum large-signal loading, is evaluated using SUPER-COMPACT for the FET chip with a net load conductance of $G_L = I_0/(V_0 - 1)$, where I_0 = drain-source current and V_0 = drain-source voltage.

Notice that both f_{MAX} and f_{3dB} (LS) depend directly upon f_t. Thus, f_t should be maximized for the highest operating frequency. Notice also that although the range in f_{MAX} is small (6 GHz) the range in f_{3dB} (LS) is significantly larger (9.5 GHz). This reflects the fact that the dc as well as the RF quantities determine the maximum frequency for useful operation of power FET's.

The largest values of f_{3dB} (LS) occur most frequently for the FET's with Fukui pinchoff voltages in the range of 3 to 5 V. Four devices with pinchoff voltages near 6 V have significantly lower values of f_{3dB} (LS). There is no apparent correlation between f_{3dB} (LS) and $N \cdot a$ product or N value. The value of f_{MAX} of the device from wafer

B1271 is exceptionally high primarily due to the exceptionally small value of drain–gate capacitance.

To evaluate the influence of each FET parameter upon performance, calculations were made of the MAG at 20 GHz for parameter changes of 0, +25 percent, and −25 percent for device B1824-20C. Fig. 10 shows the results of this study. The largest improvement (2.0 dB) occurs for increased transconductance (g_m). The decrease in transit-time (τ_t) or drain–gate capacitance (C_{dg}) improves the MAG by about 0.8 and 0.9 dB, respectively. An increase in R_{ds} or a decrease in R_d, R_g, or R_i all result in less than 0.5-dB improvement. The most significant improvement in device performance will be made by increasing g_m and reducing τ_t and C_{dg}.

VIII. Conclusion

A procedure has been developed for producing equivalent circuit models for carrier-mounted GaAs FET's for both device design and diagnostic purposes. A prominent feature of this procedure is the reduction of the number of unknown element values to be determined by *S*-parameter data, by the use of dc measurements as well as zero-bias measurements. The zero-bias data are used to evaluate the circuit inductances and are taken just before the full-bias data.

It was shown that agreement for *S*-parameters does not assure agreement for the values of stability factor and MAG. Loss in the FET carrier will affect the values determined for the circuit elements which model the FET chip.

The equivalent circuit models were used to evaluate a group of GaAs MESFET's. The conduction channel parameters were calculated and the frequency response characteristics were predicted.

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